



OPENROAD 3 YEARS IN PERSPECTIVE

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- Tom Spyrou has worked for over 30 years as an EDA Technologist and has gained extensive experience in areas including Static Timing Analysis, Logic Synthesis, Power Grid Analysis, Database Technology and Floor-planning. He has led the development of leading edge commercial engines and products such as PrimeTime, Voltage Storm, First Encounter, and the Open Access Database. Tom has been driving EDA algorithms to utilize parallel programming approaches with both multi-process and multi-threaded techniques. Tom is currently a Senior Principal Engineer at Intel in the Programmable Solutions business unit working on the Quartus FPGA compiler. He has a BS from Carnegie Mellon University in ECE and an MS from Santa Clara University.

REMEMBER WHERE WE WERE IN 2019

- The next two slides are taken from my talk in 2019 in this same forum
- A lot has changed in OpenROAD and open source EDA in general.
- Lets look at how far the effort has come
- Many thanks to all of the sponsors and team members working on OpenROAD
- The original program ends July 22 and we will continue the effort

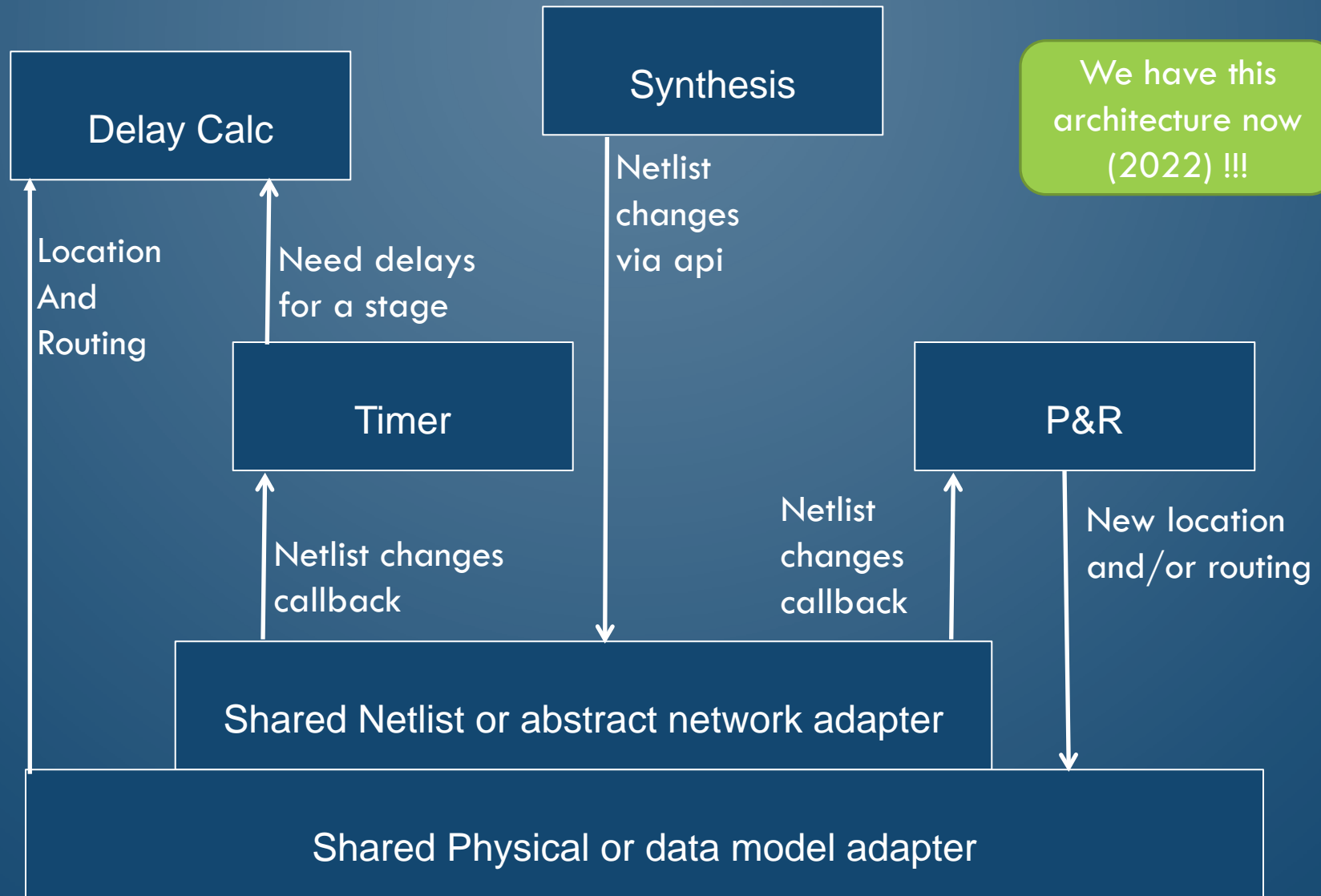
THE EDA INDUSTRY LEARNING CURVE

- Commercial EDA has gone up a learning curve regarding how to architect the complex interactions between tools in the Synthesis, Place and Route tool chain
 - Some companies like IBM went up this learning curve ahead of this time line
- 1980's - focus was on point tools connected by files
- 1990's – pervasive timing driven steps required tight connection to timing
- 2000's – tightly coupled algorithms on a shared incremental substrate
- 2010's – Advanced node effects, parallel processing, hyper-optimization

- "OpenROAD" alpha is targeting a "1980s" file-based flow
 - Except the placer which is integrating to OpenSTA directly sharing the data model

FROM SLIDE PRESENTED AT DAC 2019

INCREMENTAL ARCHITECTURE SHARED NETLIST



OPENROAD SOFTWARE ARCHITECTURE ACCOMPLISHMENTS

- Creation of OpenDB
 - Truly open source EDA database
 - Supports incremental tool development with callbacks
 - LEF/DEF 5.8
 - Verilog instance tree
- Refactoring of all engines to work on OpenDB
- Modular architecture which is easy to add engines and features to
- Extensive regression tests integrated with Github commit process

OPENROAD ACCOMPLISHMENTS

- Support of increasingly advanced nodes
 - Global Foundries 12nm
 - Intel 16nm
 - Research PDK ASAP7
- 200 tapeouts many of which were done by first time chip designers
 - OpenROAD can create a funnel of new user to design who can graduate to bleeding edge design at the latest nodes with proprietary tools
- Improvements in all key engines
 - Macro Placement, Placement, Routing, Optimization, Clock Tree Synthesis, Power Grid Synthesis and more.
 - More than 200 tapeouts in Google Funded Sky130 shuttles
 - Many first time chip designers
- DAC 2022 Creating a funnel of new users into the semiconductor industry

THERE IS A LOT TO DO

- There is a lot to do and we welcome contributors to help
 - Small enhancements
 - Documentation
 - Major projects
 - Pick an issue and work on it as a starter project
- What is most important for us to work on next?
 - The basic system and architecture is working
 - There are a lot of features to add and improvements needed in each engine
- Contact me with areas of interest or questions
 - [aspyrou at eng.ucsd.edu](mailto:aspyrou@eng.ucsd.edu)

THERE IS GREAT POTENTIAL

- Open Source EDA Tools + Open Source PDKs
 - The overhead to getting started is low
 - Download and Go!
 - Today for \$10K you can design and get 300 packaged IC's
 - Allow small companies and first time designers to be successful
 - Create a funnel of new chip designers
- With Open Source EDA you can use unlimited licenses in experiments
 - Trial designs, Machine Learning, and more...
- Reproducible research
 - The exact PDK, tool version, tool scripts and environment can be shared